10EC077



M.Tech. Degree Examination, June 2012

Synthesis and Optimization of Digital Circuits

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions.

1	b. с.	Explain the semi-custom design.(06 MarksDiscuss 'tractable' and 'intractable' problems encountered in design of microelectronic circuits.(04 MarksWhat are pareto points? Explain the significance of pareto point, with an example. (06 Marks Explain the algorithm steps involved in DIJKSTRA algorithm.(04 Marks
2	b.	Explain the algorithm steps involved in bryantls reduction procedure(10 MarksConsider a function pair $f = (a + b)c$; $g = bcd$. Compute ROBDD with variable orde(d, a, b, c). Also represent unique table.(06 MarksExplain the following terms with respect to graph theory.i) trailii) multi – graphiii) planar graphiv) bipartite graph.(04 Marks)
3	b.	Consider the following function : $x_1 = (x + dx)$; $u_1 = [u - (3 * x * u * dx) - (3 * y * dx)];$ $y_1 = (y + u * dx);$ $c = x_1 < a;$ Write a behavioral model, using silage. (08 Marks Write a UDL/I behavioral model for finite state machine that recognizes two or more consecutive 1's in an input data stream. (06 Marks Explain the optimization techniques. (06 Marks)
4	b. с.	What are tautology? Give set of rules for simplifying the recursive procedure.(06 MarksConsider the function $f = ab + ac + ab' c' + a'$. Represent this function, using positional cube notation. Verify the above function for tautology.(04 MarksGive ESPRESSO minimizer algorithm.(06 MarksConsider the function : $(\alpha) (\alpha + \beta) (\beta + \gamma) (\gamma + \delta) (\delta) = 1$ (06 MarksRepresent prime implicant table. Solve the above function by applying Petrick's method. (04 Marks)
5	a. b.	Explain the Algebraic division, with an example. Write the pseudo code for the method. (06 Marks) Find the minimum cover for the following function, using exact logic minimization algorithm $f = \Sigma m_0, m_2, m_4, m_6, m_8, m_{10} m_5, m_7, m_9, m_{11}, m_{13}$
		Represent the minimal cover on three dimensional cube. (10 Marks

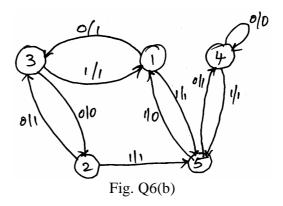
c. Give four major steps of expand procedure of logic minimization. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

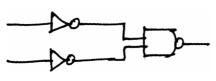
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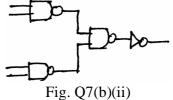
(10 Marks)

- **6** a. Explain the different types of finite state machine decompositions.
 - b. For the finite state machine Fig. Q6(b), obtain the minimum state diagram. (10 Marks)



- 7 a. Explain Hu's algorithm.
 - b. For the given cell library in Fig. 7(b)(i) and Fig. Q7(b)(ii). Write pattern arrays and pattern strings. (04 Marks)





- Fig. Q7(b)(i) c. Explain loop folding.
- d. Explain ALAP scheduling under latency constraints.
- **8** Write short notes on :
 - a. Anti fuse based FPGA
 - b. TREE BASED covering
 - c. LEFT edge algorithm
 - d. Boolean relation minimization.

(20 Marks)

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(06 Marks) (04 Marks)

(06 Marks)